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METHOD OF MOUNTING IC CHIP (English)
Patent Assignee: SEMICONDUCTOR ENERGY LAB
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JP 4295090	A2	19921020	JP 9158825	A	19910322	
JP 4295091	A2	19921020	JP 9158826	A	19910322	
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MOUNTING METHOD FOR CHIP OF SEMICONDUCTOR INTEGRATED CIRCUIT AND ELECTRONIC EQUIPMENT MOUNTED THEREWITH

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ABSTRACT

PURPOSE: To provide a COG type semiconductor integrated circuit chip mounting method wherein a defective chip can be replaced for repair.
CONSTITUTION: A semiconductor integrated circuit chip and a wiring are electrically connected together through the intermediary of projections (bumps) or conductive particles on the lead-out electrodes of the chip or the electrode wiring on a board, wherein organic resins different in setting condition such as photosetting, thermosetting, or naturally setting resin are combined and mixed together into an organic resin mixture, the resin mixture is used in a tentative bonding process, it is checked that a defective part is present or not, and a defective semiconductor integrated circuit is replaced with a new one by removing organic resin.